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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/392,034
Filing Date: September 08, 1999
Appellant(s): GONZALEZ ET AL.

Katherine A. Hamer
Reg. No. 47,628
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 23, 2005 appealing from the Office action mailed September 14, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

Appellant's brief presents arguments relating to objections of the Specification, drawing and claims, items A.1 to A.6. This issue relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,097,072	Omid-Zohoor et al.	8-2000

5,387,540	Poon et al.	2-1995
6,184,108	Omid-Zohoor et al.	2-2001

S. Wolf, "Silicon Processing for the VLSI Era, Process Integration". Vol. 2, Lattice Press 1990, pp. 54-56.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "rounding the top edge of the trench" by thermally grown oxide from the substrate, does not reasonably provide enablement for *rounding the top edge of trench* by deposition of a composition of matter on the trench surface. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The specification clearly indicated that the rounding of the edge at the top of the isolation trench is a result of thermal oxidizing of the sidewall 50 to form the insulation liner 30. (See page 12, 1st paragraph). Further, as an alternative, the insulation liner can be formed by CVD (chemical vapor deposition).

It is well known in the art that, rounding of the corner is a result of thermal oxidation that forms the sidewall liner because in the oxidation process, silicon of the substrate is oxidized to form silicon oxide, while the corner of the trench, area under the oxidation mask, is rounded by the same oxidation reaction. The sidewall liner forms by deposition, however, only deposit silicon oxide onto a surface without reacting with the silicon substrate. Since silicon of the substrate is consumed by the deposition process, the rounding of the corner does not take place.

Claim 23 specifically recites: wherein forming said liner upon said sidewall of each isolation trench comprises *deposition of a composition of matter*.

Although the specification discloses two processes, thermal oxidation or deposition, that can result in the formation of a sidewall liner. However, as discussed above, only thermal oxidation results in rounding of the top edge of the isolation trench.

The specification *fails to provide support* for rounding the top edge of the trench by deposition of a composition of matter (CVD).

How can the edge of trench be rounded when the liner is formed by deposit ?

Rounding the top edge of the isolation trench by deposition is clearly a new matter.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9, 10, 12, 13, 26 and 27 are further rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 9, 10, 12, 13, 26 and 27 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification filed September 8, 1999. In the specification, page 14, lines 14-25, applicant has stated "*Figure 7A illustrates a subsequence step of formation of the isolation trench wherein insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process. Preferably, planarization will be selective to isolation film 36, and relatively slightly selective to insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to be slightly selective to spacer 28 over insulator island 22.*", and this statement indicates that the invention is different from what is defined in the claim(s) because said passage means: **isolation film 36 is etch faster than the insulator island 22**, by a ratio of 2 to 1; 1.3 to 1; 1.7 to 1 and 1.5 to 1, while claim 9 recites: "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said *first dielectric layer* (insulator island 22) ***faster than said conformal layer*** (isolation film 36) *and said spacers* (28) by a ratio in range from of about 1:1 to about 2:1.

Clearly, claim 9 is contradicting the disclosure, thus, fails to correspond to the scope of the invention.

Similar subject matter also recite in claims 10, 12, 13, 26 and 27.

As best understood by the examiner, the upper surface of each isolation trench is formed by an etch process using an etch recipe that etches the conformal layer 36 and spacers 29 faster than the insulator layer 22.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1**, 3-27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor et al. (U.S. Patent No. 6,097,072) in view of Poon et al. (U.S. Patent No. 5,387,540) (all of record).

With respect to claim **1**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer (340); (Fig. 3C);

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a second dielectric layer (352) over the oxide layer (340) and the first dielectric layer (344), wherein forming the second dielectric layer (352) includes forming the second

dielectric layer (352) over and in contact with the exposed oxide layer (340) at the plurality of areas; (Fig. 3G);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer (352), wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas; (Fig. 3H);

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench (360) is adjacent to and below the pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench (360) has a top edge; (Fig. 3I);

filling each isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer (364), and the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364); (Fig. 3J); and

planarizing the conformal layer (364) beginning with the upper surface contour of the conformal layer (364) and extending at least to the first dielectric layer (344) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces;

wherein the conformal layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a liner upon a sidewall of each isolation trench.

However, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench etching process. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch.

This well known process is taught by the reference to Wolf page 55.

With respect to claim 3, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate. (See Fig. 4).

With respect to claim 4, the liner of Poon comprises deposition of a composition of matter (50). (See Fig. 11).

With respect to claim 5, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of further includes forming a doped region below the termination of each isolation trench.

However, Poon further teaches forming a doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further form a doped region below the termination of each isolation trench within the semiconductor substrate of Omid-Zohoor as taught by Poon to prevent the inversion.

With respect to claim 6, the upper surface for each isolation trench (376) of Omid-Zohoor is formed by CMP. (See Fig. 3M, col. 4, ll. 47-62).

With respect to claim 7, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench is adjacent to and below the pair of the spacers (356) and is situated at the corresponding area of the plurality of areas;

filling each the isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with the corresponding pair of the spacers (356), wherein filling is performed by depositing the conformal layer and the depositing is carried out to the extent of filling each of the isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) to a first thickness of the conformal layer (364) relative to the spacers (356) and the first dielectric layer (344);

planarizing the first thickness of the conformal layer (364) to a second thickness to form therefrom an upper surface for each of the isolation trench (360) that is co-planar to the other upper surfaces, wherein:

the conformal layer (364) comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches (360);

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench, each upper surface being formed from the conformal layer (364) and the spacer (356) and being situated above the oxide layer (340); and

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the oxide layer (340). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of rounding the top edge of each isolation trench.

However, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench etching process and rounding the top edge of the trench at the same time. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch. The formation of the liner (28) of Poon, by thermal oxidation inherently result in rounding of the top edge of the trench.

With respect to claim 8, the method of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

With respect to claims 9 and 10, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed in an etch process using an etch recipe that etches the conformal layer (372) faster than the first dielectric layer (344).

With respect to claim 11, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed including:

chemical mechanical planarization, CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; (Fig. 3M); and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer (340). (Fig. 3N).

With respect to claims 12 and 13, as best understood by the examiner, the etch that forms a second upper surface is well known in the art to etch the first dielectric layer (344) faster than the conformal layer (364) and the spacers (356).

With respect to claim **14**, as best understood by the examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer (340);

selectively removing the silicon nitride layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer (340) and the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming a first silicon dioxide layer (252) on and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer (352), wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the silicon nitride layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into and terminating within the semiconductor substrate (120), wherein each isolation trench (360) is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

filling each isolation trench (360) with a conformal second silicon dioxide layer (364), the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second silicon dioxide layer (364), and the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and the silicon nitride layer (344); and

selectively removing the conformal second silicon dioxide layer (364) and the spacers (356) to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the oxide layer (340), wherein the conformal second silicon dioxide layer is an electrically insulative extends continuously between and within the plurality of isolation trenches, and wherein the selectively removing is performed in the absence of masking the conformal second dioxide layer (364) over each isolation trench. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of forming a corresponding electrically active region below the termination of each isolation trench within the semiconductor substrate and forming a liner upon the sidewall of each isolation trench.

However, Poon further teaches forming a corresponding electrically active region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12) to prevent invertion. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form an electrically active region below the termination of each

isolation trench within the semiconductor substrate of Omid-Zohoor as taught by Poon to prevent the inversion.

Poon further teaches that it is well known in the art to form a liner (28) upon the sidewall of each isolation trench, the liner is confined within each isolation trench and extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench (22) wthin the semiconductor substrate (12) to remove damage caused by the trench etching process. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench etching process.

With respect to claim 15, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 16, the liner of Poon is also composed of silicon nitride (50).

With respect to claim 17, the process of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (Fig. 3O); and

forming a gate oxide layer (380) upon the portion of the surface of semiconductor substrate (120). (See Fig. 3P).

With respect to claims **18** and **24**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein forming the second dielectric layer (352) includes forming the second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein filling is performed by depositing the conformal third layer (364), and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein the conformal third layer (364) is an electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein planarizing the conformal third layer (364) to form therefrom the upper surface for each isolation trench that is co-planar to the other upper surface further comprises planarizing the conformal third layer (364) and each spacers (356) to form therefrom the co-planar upper surfaces, and planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench; (see Figs. 3L-M); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly disclosing removing the polysilicon layer along with the first dielectric layer to expose the oxide layer and rounding the top edge of each isolation trench.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended to form the spacers (356) on the thermally-grown oxide layer (340), thus, implicitly, the polysilicon layer has been removed to expose the oxide layer (340). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the

oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to rounding the top edge, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench etching process and rounding the top edge of the trench at the same time. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch. The formation of the liner (28) of Poon, by thermal oxidation inherently result in rounding of the top edge of the trench.

With respect to claim 19, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed by CMP.

With respect to claim 20, a similar reasoning as that of claim 5, a doped region below the termination of each isolation trench, is also applied here.

With respect to claim 21, the process of Omid-Zohoor '072, in view of Poon, further comprises: prior to filling each isolation trench with the conformal third layer (364), forming a liner (28) upon the sidewall of the isolation trench to remove damage caused by the trench etch, the liner (28) being confined preferentially within each isolation trench (Fig. 4) and extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate, and wherein the conformal third layer (364) is composed of electrically insulative material.

With respect to claim 22, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 23, as best understood by the examiner, forming the liner upon the sidewall of the isolation trench of Poon also comprises deposition of a composition of matter (50).

With respect to claim **25**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench; (see Fig. 3L-M);

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein the conformal third layer comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Fig. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly disclosing removing the polysilicon layer along with the first dielectric layer to expose the oxide layer and rounding the top edge of each isolation trench.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended to form the spacers (356) on the thermally-grown oxide layer (340), thus, implicitly, the polysilicon layer has been removed to expose the oxide layer (340). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to rounding the top edge, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench etching process and rounding the top edge of the trench at the same time. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as

taught by Poon to remove the damage caused by the trench-etch. The formation of the liner (28) of Poon, by thermal oxidation inherently result in rounding of the top edge of the trench.

With respect to claim **26**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) by an etch using an etch recipe that etches the first dielectric layer (344) slower than the conformal third layer (364) and the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

wherein the conformal third layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364) and the plurality of isolation trench. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly disclosing removing the polysilicon layer along with the first dielectric layer to expose the oxide layer and rounding the top edge of each isolation trench.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended to form the spacers (356) on the thermally-grown oxide layer

(340), thus, implicitly, the polysilicon layer has been removed to expose the oxide layer (340). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to rounding the top edge, Poon teaches that it is well known in the art to form a thermal liner (28) on the etched trench surface to remove damage caused by the trench etching process and rounding the top edge of the trench at the same time. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench-etch. The formation of the liner (28) of Poon, by thermal oxidation inherently result in rounding of the top edge of the trench.

With respect to claim 27, as best understood by the examiner, in the planarizing of the conformal third layer (364), the conformal third layer (364) is removed faster than the first dielectric layer (344). (See Fig. 3M).

With respect to claim **31**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a silicon nitride layer (344) upon the polysilicon layer;

selectively removing the silicon nitride layer (344) to exposed the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the pad oxide layer and over the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming the first silicon dioxide layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer (356) is situated upon the pad oxide layer, is in contact with the silicon nitride layer (344) and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the silicon nitride layer (344); and

planarizing the conformal second layer (364) and each of the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface

and is situated above the pad oxide layer (340), wherein the planarizing is performed in the absence of masking the conformal second layer (364) over each of the isolation trenches; (see Figs. 3L-M);

wherein the conformal second layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly disclosing removing the polysilicon layer along with the first dielectric layer to expose the oxide layer; forming a doped region in the isolation trench and forming sidewall liner to round the top edge of each isolation trench.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended to form the spacers (356) on the thermally-grown oxide layer (340), thus, implicitly, the polysilicon layer has been removed to expose the oxide layer (340). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to forming a corresponding doped region below the termination of each isolation trench within the semiconductor substrate, Poon further teaches forming a corresponding doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12) to prevent inversion. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form an electrically active region below the termination of each isolation trench within the semiconductor substrate of Omid-Zohoor as taught by Poon to prevent the inversion.

Poon further teaches that it is well known in the art to form a liner (28) upon the sidewall of each isolation trench, the liner is confined within each isolation trench and extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate (12) to remove damage caused by the trench etching process and rounding the top edge of the isolation at the same time. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Poon to remove the damage caused by the trench etching process and rounding the top edge.

With respect to claim 32, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 33, as best understood by the examiner, the liner of Poon is also composed of silicon nitride (50) and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 34, as best understood by the examiner, the method of Omid-Zohoor further comprises: (also see claim 25):

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (see Fig. 3N);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120); (see Fig. 3P);

forming between the isolation trenches (360), and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surfaces. (See Fig. 3N).

4. Claims **35**-40, **42** and **43** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Wolf *Silicon Processing for the VLSI Era*, Vol. 2, pp. 54-55 (of record).

With respect to claim **35**, as best understood by the examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll.14-16);

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) and the polysilicon layer to expose the oxide layer at a plurality areas;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first layer (344);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by

planarizing in the absence of masking the second layer over each of the isolation trenches; (see Figs. 3L-M); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly disclosing removing the polysilicon layer along with the first dielectric layer to expose the oxide layer and the top edge of the isolation trench being rounded.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended to form the spacers (356) on the oxide layer (340), thus, implicitly, the polysilicon layer has been removed to expose the oxide layer (340). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

With respect to the top edge of isolation trench being rounded, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the trench liner on the surface of trench (360) of Omid-Zohoor

'072 as taught by Wolf to remove damage caused by the trench etching process. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

With respect to claim 36, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type (n-type) to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 2-37).

With respect to claim 37, the doped trench bottom of wolf has a width which is greater than the width of the respective isolation trench. (See Fig. 2-37).

With respect to claim **38**, as best understood by the examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon; (Fig. 3B);

forming a first layer (344) upon the oxide layer (340); (Fig. 3C);

selectively removing the first layer (344) to expose the oxide layer (340) at a plurality of areas; (Fig. 3E);

forming a plurality of isolation trenches (360) through the oxide layer (340) at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344); (Fig. 3H);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356); (Fig. 3I);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356), wherein the filling is performed by depositing the second layer (364), and the depositing is carried out to the extend of filling each isolation trench and extending over the spacer (356) and over the first layer (344); (Fig. 3J);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340); wherein the planar upper surface is formed by planarizing in the absence of masking the second layer (364) over each of the isolation trench; (Fig. 3M); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of disclosing the top edge of the isolation trench being rounded.

However, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Wolf to remove damage caused by the trench etching process. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

With respect to claim 39, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type (n-type) to form a doped trench bottom that is below and in contact with a respective one of isolation trenches. (See Fig. 2-37).

With respect to claim 40, the doped trench bottom of wolf has a width which is greater than the width of the respective isolation trench. (See Fig. 2-37).

With respect to claim **42**, As best understood by examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer; (col. 4, ll. 14-16);

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers (356) of the respective first and second isolation structures (360), wherein filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trenches and extending over the spaces (356) and the first layer (344); and

forming with a single etch recipe a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of disclosing the top edge of the isolation trench being rounded.

However, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Wolf to remove damage caused by the trench etching process. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

With respect to claim **43**, as best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer (344);

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and

a second spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously

therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of filling each isolation trench and extending over the spaces (356) and the first layer (344); and

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of respective first and second isolation structures, and being situated above the oxide layer, wherein planarizing is performed in the absence of making the conformal layer over each of the isolation trenches, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of disclosing the top edge of the isolation trench being rounded.

However, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench by forming a thermal liner.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Wolf to remove damage caused by the trench etching process. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

(10) Response to Argument

Non-Appealable Subject Matter:

The non-appealable subject matters will not be addressed at this time pending the outcome of the appealable subject matters from the Board.

Rejection under 35 U.S.C. 112, first paragraph:

Appellant appears to contend that claim 23 uses the transitional phrase "comprising" not "consisting of" therefore other action can be further performed within the scope of the claim.

As discussed in detail previously, the specification clearly discloses that the sidewall liner instead of being formed by thermal oxidation, can be alternatively formed by deposition, which means either formed by thermal oxidation or deposition, but not both.

Claim 18, in which claim 23 depends on, have already claimed : "rounding the top edges of each said isolation trench", which means the sidewall liner is already formed by thermal oxidation thus, result in rounding the top edge of the isolation trench.

Claim 23 recites: wherein forming said liner upon said sidewall of each isolation trench comprises deposition of a composition of matter.

Since the sidewall liner has already been formed by thermal oxidation, then claim 23 now directed to unsupported new matter, additionally formed by deposition.

Secondly, Appellant also appears to contend that rounding the top edges of the isolation trench can be made by deposition of matter.

As discussed above, rounding of the top edge of the isolation trench is the direct result of thermal oxidation, while deposition does not consume silicon from the substrate, thus, the top edge can not be rounded.

Appellant fails to show the deposition results in rounding of the top edge. Thus, the rejection should be maintained.

Rejection under 35 U.S.C. 112, second paragraph:

Appellant argues that the specification supports the claimed subject matter of claim 9, 10, 13, 26 and 27 that the isolation film 36 in the figures is etched slower than the insulator island.

However, the argument only correct when the later process steps that removing the insulator island, but at the process step of removing the conformal layer, as claimed, this statement is incorrect. According to the specification, there are two process steps that involve etching. The first etching is the planarization of the conformal layer 36 (claimed) and the second etching is the removal of the insulator island 22 (not claimed).

In the first etching, the target is planarizing the conformal layer 36 and the island 22 is the etch stop. In this process step, the etch rate of the conformal layer 36 is removed faster than that of the island 22. As shown in Figs. 6A to 7A.

In the second etching, the target is the island 22 and the remaining of layer 36, the spacer 28 and pad oxide 14 are the etch stop. In this process step, the etch rate of the island 22 is removed faster than that of the oxide 36, 28 and 14. As shown in Figs. 7A to 8A.

Claim 9 recites: a method of claim 7, wherein said upper surface of each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer

(island 22) *faster* than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1. (Emphasis added).

In claim 7, the etching that forms the upper surface is the planarization to remove the conformal layer 36. This process step requires the removal rate of the conformal layer to be faster than the etch stop (island 22). The specification, page 14, lines 19-21, states: "the inventive method is in the range of about 1:1 to about 2:1 selective to isolation layer 36 as compared to insulator island 22" which means the isolation layer 36 is moved up to twice (2 to 1) as fast as the island 22. In this process, as discussed above, conformal layer 36 is removed faster than the insulator island 22, not other way around.

Appellant appears to invent the term "selective" as to means "slower".

In the specification, there are two occurrences of "selective to isolation film 36". The first occurrence, on page 4, line 17, is to etch the conformal layer 36 and the second occurrence, page 17, line 15 , is to remove the island 22. If "selective" means "slower" then in both etch steps, the conformal layer 36 does not remove at all.

Clearly, these claims contradicting the fundamental of the process technology, the specification and the parent claims and the rejection should be maintained.

Rejection under 35 U.S.C. 103(a):

With respect to claims 1, 3-27 and 31-34, Appellant argue: the method in the '072 patent relies on the deposition on a reverse-resist mask 368 over the trench region 356.

Claim 1 recites (a)"filling each said isolation trench with a conformal layer. . . so as to define an upper surface contour of the conformal layer" and (b)"planarizing the conformal layer

beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer and each said spacer.".

The '072 clearly teaches just that:

(a) filling each isolation trench (360) with a conformal layer (364). . . so as to define an upper surface contour of the conformal layer. (See Fig. 3J).

(b) planarizing the conformal layer (364) beginning with the upper surface contour of the conformal layer (Fig. 3K) and extending at least to the first dielectric layer (344) and each said spacer (356). (See Figs. 3K-3M).

The term "planarizing" means a etching, as clearly indicated in the specification. From Fig. 3K, the etching clearly beginning with the upper surface contour of the conformal layer (364). Appellant's argument with respect to the reverse-resist mask is irrelevant because clearly, claim 1 does not exclude the use of any mask.

With respect to claim 7, Appellant argues: the method disclosed in the '072 patent does not teach or suggest planarizing the first thickness of the conformal layer to a second reduced thickness".

Form Fig. 3J of '072 patent, the isolation trench (360) clearly is filled to a first thickness relative the spacers (256) and the first dielectric layer (344), and planarizing the first thickness of the conformal layer (364) to a second reduced thickness (376). (Fig. 3M).

Again, the Appellant's argument with respect to the mask is also irrelevant.

With respect to claim 18 and 24-26, Appellant argue that the '072 patent discloses a method that involves masking and etching a conformal layer prior to planarizing the layer.

Claims 18 and 24-26 recite: "selectively removing said conformal second silicon dioxide layer....and wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over said isolation trench".

From Figs. 3L to 3M, during the selectively removing of the conformal layer (364) there is no masking involve.

Claims 18 and 24-26 clearly fail to exclude the use of mask prior to "selective removing".

Therefore, the dependent claims 3-6, 8-17, 19-23 and 27 are obvious over '072 patent in view of Poon.

With respect to claim 31, Appellant argues: the method disclosed in the '072 patent does not planarize the conformal oxide layer to produce the structure with an upper surface for each isolation trench. Instead, the '072 patent relies upon a more complicated method with more steps.

Instead of pointing out the limitations of the claim that the '072 patent fails to teach, Appellant argues that a more complicated method with more steps are used.

From Fig. 3L to 3M, the '072 patent clearly teaches planarizing the conformal second layer (364) to produce the structure with an upper surface for each isolation trench and does so without a mask.

The '072 patent clearly teaches all limitations that the Appellant alleges missing, thus, the combination in view of Poon, clearly rendered claim 31 and it dependent claims obvious.

With respect to claims 9, 10, 12, 13, 23 and 27, beside from indefiniteness and enablement as discussed above, these claims depend on the rejected independent claims 7, 18 and 26 which have been deemed obvious over the '072 in view of Poon. The rejection of these claims should be maintained as well.

With respect to claim 34, the '072 patent clearly teaches a layer composed of polysilicon, col. 4, lines 14-16, upon the so called gate oxide layer in contact with the pair of the spacers, and selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surfaces. (See Figs. 3M-3N).

With respect to claim 35, the Appellant appears to contend that, the '072 patent does not teach "forming a polysilicon layer upon said oxide layer".

However, the '072 patent, col. 4, line 14-16, clearly teaches: "Also, a pad oxide containing a thin thermally-grown oxide layer and a buffer polysilicon layer may be used for the pad oxide 340". Moreover, the planarization of the '072 patent is performed in the absence of masking of the conformal layer over each of the trench, as shown in Figs. 3L-3M.

With respect to claim 43, again the Appellant contends that the '072 patent relies upon a more complicated method with more steps and does not planarize the conformal oxide layer 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein.

As discussed above, the limitations of claim 43 do not exclude any simple or complicated methods to form a planar surface. Fig. 3M of the '072 patent speaks for itself, that a planar surface has been achieved.

With respect to claim 42, similarly, the Appellant contends that the '072 patent utilizes a more complicated method to have a planar surface.

Again, from Fig. 3L, there is only one etch recipe to form the planar surface as shown in Fig. 3M. Thus, there is no deficiency as alleges.

With respect to claims 36, 37, 39 and 40, these claims depend on the rejected claims 35 and 38, and also have been determined to be obvious over the cited references.

The rejection of these claims should be maintained as well.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Anh D. Mai

Conferees:

Mr. Ricky L. Mack, SPE. Ricky Mack

Mr. Wael M. Fahmy, SPE. W.F